What is claimed is:

[Claim 1] 1. A method of modifying circuit design source data of a three-dimensional structure for improving integrated circuit yield, comprising the steps of:

spreading wires using a post-routing layout optimizer;

locating a problem structure remaining after post-layout optimizing using a shapes-processing tool; and

implementing at least one local modification to said three-dimensional structure to perform a fix-up process on the problem structure.

[Claim 2] 2. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises increasing the flexibility of at least one wire of an Mx layer passing over an incompatible structure component of the problem structure.

[Claim 3] 3. The method of claim 2, wherein increasing the flexibility of at least one wire comprises inserting at least one jog in the at least one wire.

[Claim 4] 4. The method of claim 1, further comprising locating a problem structure using a shapes-processing tool.

[Claim 5] 5. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises increasing a space between at least two wires on a layer over an incompatible structure component of the problem structure.

[Claim 6] 6. The method of claim 5, wherein increasing a space between at least two wires comprises forming a dummy shape between the at least two wires and increasing the size of the dummy shape.

[Claim 7] 7. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises

forming a dummy hole in an incompatible structure component of a first layer of the problem structure to reduce manufacturing defects of a structure component in a second layer of the problem structure.

[Claim 8] 8. The method of claim 7, wherein forming a dummy hole comprises forming a gap in the incompatible structure.

[Claim 9] 9. The method of claim 1, wherein implementing at least one local modification to a ground-rule to perform a fix-up process comprises causing a router to reroute at least one wire.

[Claim 10] The method of claim 8, wherein implementing at least one design tool to perform a fix-up process comprises widening a trench of a Mx-1 layer of the problem structure under at least one wire of a Mx layer of the problem structure.

[Claim 11] 11. A method of modifying circuit design source data for forming a multi-layer structure of a semiconductor device, comprising the steps of:

determining whether at least two minimum-spaced wires of an upper layer pass over a dishing-prone structure of a lower layer; and if so performing at least one of:

increasing a space between the two minimum-spaced wires of the upper layer in a region over the dishing-prone structure of the lower layer, forming a dummy hole in a wide wire under the space between the two minimum-spaced wires; and

widening a trench between two wide wires under the space between the two minimum-spaced wires.

[Claim 12] 12. The method of claim 11, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires above the dishing-prone structure.

[Claim 13] 13. The method of claim 12, wherein increasing the flexibility of the at least one wire of the two minimum-spaced wires comprises forming at least one jog in the at least one wire.

[Claim 14] 14. The method of claim 11, wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two wide wires by increasing the width of the dummy shape.

[Claim 15] 15. The method of claim 11, wherein forming the dummy hole in the wide wire comprises forming a gap configured to be filled with a dielectric in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires.

[Claim 16] 16. The method of claim 11, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires.

[Claim 17] 17. The method of claim 11, wherein widening the trench under the space between the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires.

[Claim 18] 18. A method of modifying circuit design source data of a three-dimensional structure for forming a multi-layer structure of a semiconductor device, comprising the steps of:

forming a dishing-prone structure on a lower layer;

forming two minimum-spaced wires over the dishing-prone structure on an upper layer;

increasing a space between the two minimum-spaced wires in a region over the dishing-prone structure;

if the dishing-prone structure includes a wide wire, inserting a space for a dielectric island in the wide wire under at least one wire of the two minimum-spaced wires; and

if the dishing-prone structure includes a narrow trench between two wide wires, widening the narrow trench under of the space between the two minimum-spaced wires.

[Claim 19] 19. The method of claim 18, further comprising increasing the flexibility of at least one wire of the two minimum-spaced wires proximate the dishing-prone structure.

[Claim 20] 20. The method of claim 19, wherein increasing the flexibility of the at least one wire comprises forming at least one jog in the at least one wire of the two minimum-spaced wires.

[Claim 21] 21. The method of claim 18, wherein increasing a space between the two minimum-spaced wires comprises forming a dummy shape between the two minimum-spaced wires and increasing the width of the dummy shape.

[Claim 22] 22. The method of claim 18, wherein forming a dielectric island configured to be filled with a dielectric in the wide wire comprises forming a gap in the wide wire approximately perpendicular to a long axis of the at least one wire of the two minimum-spaced wires.

[Claim 23] 23. The method of claim 18, further comprising causing a router to reroute at least one wire of the at least two minimum-spaced wires.

[Claim 24] 24. The method of claim 18, wherein widening the narrow trench under at least one wire of the two minimum-spaced wires comprises narrowing at least one wide wire of the two wide wires.

[Claim 25] 25. Circuit design source data for a multi-layer structure of a semiconductor device, comprising:

an upper layer comprising multiple minimum-spaced wires;

a lower layer comprising a dishing-prone structure, wherein the multiple minimum-spaced wires of the upper layer are disposed over the dishing-prone structure of the lower layer;

an increased space between at least two wires of the multiple minimum-spaced wires in a region over the dishing-prone structure;

a dummy hole in the wide wire under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a wide wire; and

a widened region of the narrow trench under at least one wire of the multiple minimum-spaced wires if the dishing-prone structure includes a narrow trench between two wide wires.

[Claim 26] 26. The circuit design data of claim 25, comprising a jog in at least one wire of the multiple minimum-spaced wires proximate the dishing-prone structure.

[Claim 27] 27. The circuit design data of claim 26, comprising at least two jogs in at least one wire of the multiple minimum-spaced wires proximate the dishing-prone structure.

[Claim 28] 28. The circuit design data of claim 25, wherein an increased space between at least two wires of the multiple minimum-spaced wires comprises an adjustable shape between the at least two wires of the multiple minimum-spaced wires.

[Claim 29] 29. The circuit design data of claim 25, wherein the adjustable shape in the wide wire comprises a gap in the wide wire approximately perpendicular to a long axis of the at least one wire of the multiple minimum-spaced wires.

[Claim 30] 30. The circuit design date of claim 25, wherein a widened region of the narrow trench comprises a narrow region of at least one wide wire of the two wide wires.